History of Instruction Sets

By Kyle Malaguit and Lucas Saca

Just what is this *instruction set architecture?*

The complete set of all the instructions in machine code that can be recognized and executed by a central processing unit.

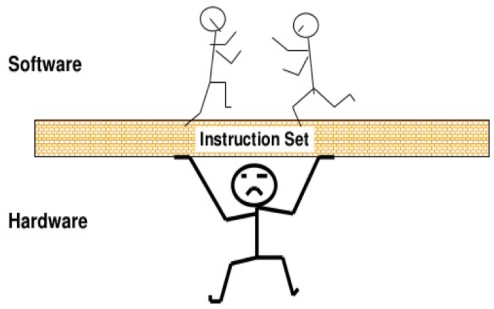
It defines all programmer-visible components and operations on the computer

- Memory space
- Registers
- Instruction sets

What makes them different?

Instruction sets vary in…

- Bit size
- Max operands
- Use of memory and/or registers
- Chip design
- Number of registers
- Instruction Encoding
- Branch Evaluation
- Endianness
- Application - desktop/server versus embedded



Source: Computer Architecture: A Quantitative Approach, J. L. Hennessy & D. A. Patterson, 3rd Edition.

History of Instruction Sets

- **IBM System/360, System/370, z/Architecture (1964)**
- CDC 6000 (1964)
- Digital Equipment Corporation PDP-8 (1965)
- DEC PDP-11 (1970)
- Intel 8080 (1974)
- MOS Technology 6502 (1975)
- Zilog Z80 (1976)
- Intel 8051 [MCS-51] (1980)
- **DEC VAX (1977)**
- **Intel x86 (1978)**
- Motorola 68000 (1979)
- National Semiconductor NS320xx (1982)
- **ARM/A32 (1985)**
- **MIPS (1985)**
- Sun Microsystems/Fujitsu SPARC (1985)
- Hewlett-Packard PA-RISC (1986)
- **Inmos Transputer (1987)**
- DLX (1990)
- **IBM POWER, PowerPC, Power ISA (1990)**

History of Instruction Sets

- DEC Alpha (1992)
- Hitachi SuperH [SH] (1994)
- ARM Thumb/T32 (1994)
- ARC International - ARC (1996)
- Atmel AVR (1997)
- MMIX (1999)
- Analog Devices Blackfin (2000)
- Transmeta Crusoe [native VLIW] (2000)
- Renesas Electronics RX (2000)
- Intel Itanium [IA-64] (2001)
- Sunplus Technology S+core (2005)
- Atmel AVR32 (2006)
- eSi-RISC (2009)
- OpenRISC (2010)
- RISC-V (2010)
- ARM A64 (2011)
- Elbrus VLIW (2014)

System /360, developed by IBM (1964)

- Considered the first modern instruction set
  - Series of instruction set compatible machines
- Successes attributable to Gene Amdahl
- Ushered in an era of computer compatibility
  - Allowed machines across a product line to work together
- Pioneered 8-bit byte
- 6 processor models and 54 peripheral devices
  - magnetic storage devices, visual display units, communication equipment…

You know what they say

The Pioneers used to ride these babies for miles

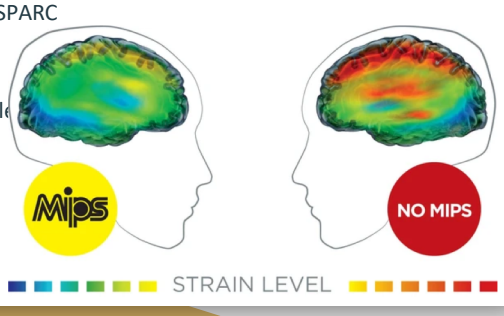
1. 8-bit byte
2. Byte addressable memory
3. 32-bit words
4. Variable length instructions
5. Two's complement arithmetic
6. Segmented and paged memory
7. Commercial use of microcoded CPUs
8. IBM floating point Architecture
9. Extended Binary Coded Decimal Interchange Code
10. Offer dynamic address translation and virtual machine capabilities to its users

Instruction sets subsets

Complex Instruction Set Computer (CISC): Computers that were designed with a full set of computer instructions within its hardware. Instructions were carried out on the computer's memory bank, thus not utilizing load or storing functions. Examples include Intel's x86, Motorola's 68k, and System /360.

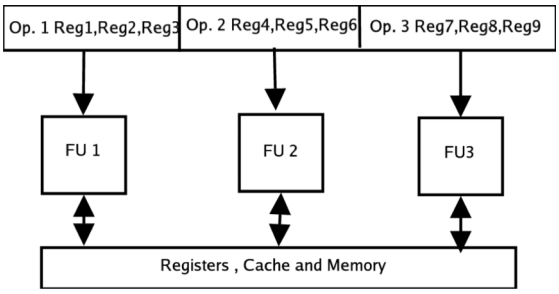
Reduced Instruction Set Computer (RISC): Most programs did not fully utilize all the instructions within a CISC. Thus, the RISC came about in the late 1970s. Ex. ARM, MIPS, SPARC

- Many instructions were removed
- Address modes were reduced
- Multi-cycle instructions were cut down to single cycle



VLIW

Very Long Instruction Words (VLIW): The concept of this architecture and its acronym was invented by Josh Fisher in the early 1980s. This architecture utilizes instruction level parallelism by having the compiler break down the program instruction into basic operations that can then be executed in parallel. Operations are faster at the cost of higher hardware overhead. Ex. Elbrus 2000, Intel's Itanium IA-64



Okay, this is EPIC

Explicitly Parallel Instruction Computing (EPIC): In 1997, the forces of Intel and HP united in order to make something truly EPIC. This led to the Itanium Architecture that holds similarities to VLIW computing. This architecture allowed software instructions to be executed in parallel by using the compiler.
Ex. Itanium series

In 2008, it was the fourth most deployed microprocessor architecture. Truly EPIC.

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Okay, this is epic

Bibliography

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